

## **PRESS RELEASE**

### **Linley Tech Seminar Highlights Developments in CPU Cores and Intellectual Property for Networking and Communications ASICs and SoCs**

MOUNTAIN VIEW, CA—January 19, 2007—On January 31, The Linley Group presents the first of its Linley Tech 2007 seminar series with "CPU Cores and IP for Networking." Architects and technologists from leading intellectual property vendors will discuss the latest technologies for networking and communications applications.

The Linley Group, the leading supplier of technology analysis for networking silicon, continues its tradition of providing independent coverage of important topics in networking-system design. The seminar is intended to provide critical information to help ASIC and system-on-a-chip (SoC) designers choose the right IP and integrate it into their designs.

The seminar will open with a CPU and IP overview by Linley Gwennap, Principal Analyst with The Linley Group, highlighting recent trends in intellectual property. The morning session, led by Joseph Byrne, senior analyst with The Linley Group, will focus on coprocessors and interface IP. The afternoon session, led by Linley Gwennap, will cover CPU Cores for ASICs and SoCs.

You won't want to miss this outstanding lineup of presenters, including:

- Mike Uhler, CTO at MIPS Technologies, will present "Improving Performance Using Multithreading."
- Satish Premanathan, Chief Architect at Wipro Technologies, speaking on "Integrating RF Technology in a Wi-Fi SoC."
- Steve Singer, Systems Engineering Manager at SafeNet, will present "Networking Security in Silicon."
- Toby Foster, System Architect at Freescale, will present "Custom ASICs Featuring PowerQUICC and StarCore Technologies."
- Sumit Gupta, Product Marketing Manager at Tensilica, will present "Networking Applications for Xtensa Configurable CPU Cores."
- Dave Steer, Director of Enterprise Solutions at ARM, will present "Implementing High-Speed Consumer Networking Using ARM."
- Harry Linzer, Senior Engineer at IBM, will present "Power CPU Cores Without All the Power."
- Prakash Rashinkar, Director of Engineering at Rambus, will present "Integration: The Hidden Cost of IP."



The seminar wraps up with a closing panel on the future directions for networking IP. Following the seminar will be a reception providing the opportunity for attendees to meet with industry leaders, distinguished speakers, analysts, designers, and their colleagues.

Admission is free to qualified individuals who register by Jan. 26. The seminar will be held at the DoubleTree Hotel in San Jose. The seminar is targeted at ASIC and SoC vendors, OEMs, press, and the financial community. This event is sponsored by Freescale, Tensilica, SafeNet, MIPS, Rambus, IBM, ARM, and The Linley Group.

For further details and registration information, visit The Linley Group web site: <http://www.linleygroup.com/seminars.html>

### **About The Linley Group**

The Linley Group, the leading provider of independent technology analysis for networking, communications, and consumer electronics semiconductors, covers emerging areas such as high-speed embedded processors, Gigabit and 10G Ethernet, wireless handset processors, access processors, security and content processors, high-speed interconnects, and more. The company provides in-depth technology reports and interactive seminars as well as strategic consulting services tailored to the individual client. To get free access to The Linley Group's analysis of recent news and events in these markets, subscribe to our e-mail newsletters. More information about The Linley Group is available at <http://www.linleygroup.com>.

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