Single-Chip Control/Data-Plane Processors
Trends, Features, Deployment

By Linley Gwennap
Principal Analyst

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This paper examines the trend toward combining control-plane and data-plane processing on a single chip. It discusses the technologies driving this trend, the common features of these chips, their advantages and disadvantages, and how they are being deployed today and into the future.

What Is an SCDP?

A single-chip control/data-plane processor (SCDP) combines control-plane and data-plane processing on a single chip. In networking or communications equipment, the data plane processes each packet as it passes through the system. Data-plane tasks may include converting packets from one protocol to another, encrypting or decrypting data, filtering unwanted packets, prioritizing packets, and routing them to their next destination. A relatively simple processor with a small amount of software can perform these tasks, but they must be done quickly. Packets must be processed at least at wire speed, that is, the speed of the incoming network connection (e.g., 1Gbps for a Gigabit Ethernet connection).

The control plane handles packets that require extra processing, typically about 5% to 10% of all packets. The most common example is a routing update (e.g., RIP, BGP); the control plane maintains the route table. The control plane may also process other protocols (e.g., ARP) that are too complex for the data plane, or legacy protocols (e.g., SNA, AppleTalk) that are rarely encountered. Finally, the control plane also handles management tasks such as system configuration and logging.

Because of the differing characteristics of control-plane and data-plane processing, these two tasks have typically been performed on separate chips. The control plane typically uses a general-purpose processor, which is easy to program and can handle large amounts of code. To attain wire speeds of 1Gbps or more, the data plane may use a device such as an ASIC, an FPGA, or a network processor (NPU). These specialized devices increase throughput and reduce power dissipation compared with a general-purpose processor.

With IC process technology reaching 65nm, 45nm, and below, the transistor budgets for leading-edge devices are growing rapidly. These budgets can easily accommodate multiple processors on a single chip, along with associated coprocessors and system interfaces. Thus, Moore’s Law is driving the integration of the control plane and data plane into a single device: the SCDP. This integration will occur first at the low end, where the processors require less die area and can more easily be combined, and move upward toward the high end as transistor budgets increase.
**Ideal Characteristics**

**Control Plane**

For the control plane, the SCDP needs a powerful CPU compatible with one of the leading instruction sets, such as Power, x86, or MIPS. For any of these standard architectures, a broad range of software-development tools is available to ease the programming task. In many cases, the customer already has control-plane software for a particular application and wishes to reuse it with minimum porting effort. In network routers and communications equipment, the most popular instruction set for control-plane software is Power, which is supported by leading OEMs such as Cisco, Juniper, Nortel, Siemens, and Alcatel-Lucent.

Control-plane software has fewer computations and more conditional branches than typical applications. Thus, it will perform better on CPUs with a short pipeline (small branch misprediction penalty). CPUs with a longer pipeline will gain some benefit from sophisticated branch-prediction techniques.

The performance requirement of the control-plane CPU depends mainly on the wire speed. A system with a throughput of 10Gbps might need a 1GHz control-plane CPU, assuming typical packet sizes and percent of control-plane packets. If the CPU needs to do exception processing or other functions, the performance requirement increases. Because most high-end CPUs top out at 2GHz–3GHz, systems with throughputs of 20Gbps or greater often require multiple CPUs to share the load in the control plane. Conversely, a system with only a few Gigabit Ethernet ports can use a lower-speed CPU for the control plane.

**Data Plane**

Data-plane engines are typically specialized CPUs that lack floating-point units, SIMD units, MMUs, and even caches, because packet data is highly transient. A small local memory holds instructions, limiting the available code space, often to several thousand instructions. These engines may include special instructions to extract and manipulate fields of arbitrary bit length, as these operations are useful in some packet protocols. As with the control plane, short pipelines can be advantageous in data-plane processing. Clock rates are often modest (1GHz or less) to minimize power dissipation.

Eliminating unneeded features makes the data-plane engine compact in die area. As a result, a 45nm processor can pack more than 100 engines onto a single die, if necessary. The actual number of engines will scale with the required wire rate and the complexity of the processing required. A 10Gbps data plane, for example, might need 20 scalar packet engines at 1GHz each.

Some data-plane engines are **multithreaded**. In this approach, if CPU needs to wait for data (e.g., an access to memory), it can execute instructions from a second thread while it is waiting, improving efficiency. This technique is well suited to data-plane code, which can map each incoming packet to a different thread; since the software must already deal with multiple data-plane engines, adding multithreading is a simple extension to...
the software model. These benefits will increase the usage of multithreading in future data-plane designs.

The SCDP may also integrate hard-wired engines (sometimes called accelerators) that offload specific tasks from the control-plane or data-plane CPUs. These might include TCP/IP checksums, packet classification, segmentation and reassembly (SAR), or even complete traffic-management units. These offload engines can reduce the load on the CPUs, enabling the design to use fewer or slower CPUs to achieve the same wire speed. Because hard-wired engines are much more power-efficient than CPUs, this trade-off will reduce the overall power of the SCDP device.

More advanced processors may include offload engines for functions such as encryption, pattern matching, or RAID checksums. These engines would be useful in VPN, intrusion detection, or storage applications. These applications require more processing power than simple routing and protocol conversion, but adding offload engines can avoid the need to boost CPU performance.

**Interconnect**

The internal bus structure (generically called interconnect) for an SCDP can be quite complex. The chip may contain multiple control-plane CPUs, multiple data-plane engines, several offload engines, and various memory and I/O ports. In a simple design with only a few CPUs and engines, these units can be connected to a single bus that also connects to memory. This bus may bridge to a second, lower-speed bus that connects to I/O devices. In a more complex SCDP, the control-plane CPUs may have a separate bus from the data-plane engines, as it becomes impractical to connect more than 20 devices to a single bus.

To avoid creating a bottleneck, the throughput of these on-chip buses must be matched to the throughput of the CPUs. Specifically, the buses must handle the total amount of memory and I/O requests from all CPUs they connect to. In addition, the buses must have provision for inter-CPU communication, which may be implemented using special bus transactions or by maintaining cache coherency. In the latter case, each CPU must monitor traffic on the bus to ensure that all CPUs have access to the same data.

High-end SCDP devices may implement more complex bus structures. Many use a crossbar consisting of several parallel bus segments; this design increases bandwidth and can perform multiple transactions at a time, reducing latency. Some use point-to-point connections to form a ring; this method increases throughput but also increases latency, as many transactions require several “hops.” An alternative to a ring is a mesh, which also uses point-to-point connections but reduces the number of hops by adopting a two-dimensional structure. The mesh design enables scaling to large numbers of CPUs per chip.

**Interfaces**

An SCDP must have adequate memory bandwidth. To minimize cost, most devices use mainstream PC memory, which is DDR2 SDRAM today, shifting to DDR3 by early 2010.
The SCDP must support at least enough bandwidth to move all data into and out of SDRAM one time. Assuming 50% utilization, peak memory bandwidth should be at least four times wire speed (e.g., 40Gbps for 10Gbps wire speed). Systems targeting more than 10Gbps may require multiple 64-bit-wide memory banks. Except in SOHO, ECC protection is generally required to maintain high reliability.

Because an SCDP has multiple processors, it can benefit from having multiple memory controllers. For example, a control-plane CPU could access one bank of memory while a data-plane engine accesses another bank. This method does not increase bandwidth, but it reduces latency by supporting multiple transactions at once. It can also improve the page-hit rate for each bank, further optimizing throughput.

In high-end devices, the use of embedded DRAM can reduce external bandwidth requirements. Using embedded DRAM, designers can fit much more memory onto the processor chip than using embedded SRAM or cache memory. Keeping commonly used data items on chip can reduce external bandwidth requirements by 50% or more, reducing the number of pins required to connect to DRAM (and therefore the package cost of the SCDP) while avoiding the need for expensive specialty memory devices such as TCAM or RLDRAM.

The SCDP must have interfaces that can receive and transmit packets at wire speed. Ethernet is the interface of choice for networking and, with the emergence of carrier Ethernet, for most communications equipment as well. Thus, the SCDP should include Gigabit and/or 10G Ethernet MACs to support the desired wire speed. These can use RGMII, SGMII, or XAUI to connect to external PHY or switch chips. For non-Ethernet applications, such as broadband or legacy connections, an external controller can connect via xGMII or PCI.

To simplify system design, the SCDP should include other basic I/O such as UARTs, GPIO, and a Flash memory connection. A single USB and a single SATA port are desirable, particularly for devices targeting SMB or SOHO. Even enterprise equipment often contains a hard drive, and the USB port may be used to download firmware updates from a memory stick.

Power and cost requirements vary with the performance level. SMB systems process hundreds of Mbps and require an SCDP at less than 10W and less than $100. An SCDP for enterprise or access infrastructure equipment might consume 30W and cost up to $200 to handle up to 4Gbps. High-end equipment that processes 10Gbps or more may have a combined budget of 60W and $600 or greater.

Advantages and Disadvantages

The combination of control-plane and data-plane engines into a single device has a number of advantages. Overall performance can be improved due to tighter integration of the two components. For example, bandwidth between the two can be increased and latency reduced by using an on-chip interconnect instead of a chip-to-chip connection. Power dissipation is also reduced by this combination, again through the elimination of the chip-to-chip interface between the control and data planes. Chip-to-chip connections...
consume far more power than short, on-chip connections, particularly at the high bandwidth required to connect the control and data planes.

Integration reduces cost in several ways. Manufacturing cost of the SCDP should be lower, assuming the separate processors were pad limited or smaller than 100mm² each. Additional manufacturing cost savings come from eliminating one package and consolidating duplicate functions and pins, such as JTAG. System cost can be reduced by reducing board area and consolidating external memory arrays and other support logic.

By controlling the design of both the control and data planes, the SCDP supplier can optimize the two components to work with each other, rather than having to support third-party components. This holistic approach can provide further benefits in performance or cost savings. For example, the control plane and data plane can share the same memory structures, reducing system cost and eliminating the time required to copy data from one memory to another.

On the downside, the SCDP eliminates the possibility of combining control-plane and data-plane processors from different vendors. Although these combinations can address specific or unusual customer needs, an SCDP simplifies the customer’s design effort and provides a single point of contact to resolve any issues with the device.

For the chip supplier, an SCDP is a more complex design effort than a standalone processor, both for hardware and the associated software. A successful SCDP design will most likely be based on control-plane and data-plane processors that have already been proven in standalone versions. As SCDP products become more common, it will become increasingly difficult for a vendor to succeed in this market without both control- and data-plane expertise.

**Programming Issues**

The SCDP is likely to include multiple CPUs in the data plane and possibly the control plane as well. Such a complex architecture requires careful programming to achieve its rated performance. In a standard-product (ASSP) model, the chip supplier will generally provide some or all of the required data-plane code plus an API for the control plane. In an ASIC model, the OEM must develop its own software to match the chip design.

Programmers are best advised to assume that both the control and data planes will be multicore and code accordingly. Any design that is not multicore today is likely to move in that direction in the near future. The key questions are how to coordinate the efforts of multiple cores.

One method is to maintain cache coherency among all CPUs and run an SMP (symmetric multiprocessing) operating system across all of them. This approach is appropriate in designs that provide a sea of identical CPUs (e.g., Cavium Octeon), each of which can be assigned to control- or data-plane tasks as needed. Unfortunately, SMP operating systems will not work with data-plane engines that lack an MMU or cache coherency, and they create an overhead layer for each processor that reduces overall throughput.
An alternate method is to run a simple kernel on each data-plane engine to reduce overhead. Even in this scenario, the control-plane CPUs typically operate in an SMP fashion, as they must maintain common data structures (e.g., the routing table) and may need to access OS services.

The data-plane engines can be organized in two ways. In a parallel model, one CPU is designated as the master, receiving all packets and assigning them to engines as needed. To maintain packet order with a flow, the master CPU can preclassify the packets and assign all packets from a flow to the same engine, a technique called “flow affinity”. The remaining engines merely need to wait for a packet, process it to completion, and then wait for another packet.

Alternatively, the data-plane engines can be arranged in a pipeline. For example, the first engine could classify packets, the second could perform filtering, the third could perform encapsulations, and the fourth could perform traffic management. This arrangement may be required if the data engines have a small instruction memory that cannot hold the entire packet-processing code. It also ensures proper ordering and deterministic latency. The two methods can be combined; for example, each pipeline stage could have multiple engines working in parallel.

As noted above, some SCDP designs use a homogenous architecture consisting of identical CPUs. In this approach, all CPUs are general purpose and execute a standard instruction set. This approach provides greater flexibility, because the programmer can allocate CPUs to the control and data planes rather than having the allocation fixed in hardware, as in the traditional heterogeneous architecture. In addition, the programming tools are consistent across both control and data plane, and programming the data plane is easier than with a proprietary instruction set.

On the other hand, general-purpose CPUs are less efficient, both in die area and power dissipation, than optimized data-plane engines. For those designers willing to cope with multiple programming models, heterogeneous designs can deliver greater performance than homogeneous designs.

Offload engines present another complication to the programming model. If the data plane is divided among proprietary programmable engines (as in a heterogeneous SCDP) and hard-wired engines (such as a traffic manager), accessing the hard-wired engines is restricted to a small amount of proprietary data-plane code. If offload engines are accessed from a general-purpose CPU, either in the data plane or the control plane, the chip designer will generally provide an API to simplify access to the offloads. These APIs differ from one SCDP to another, however, so programmers choose to use these offload engines, their code will only be easily portable among SCDPs from the same vendor.

**Deployment Trends**

SCDP technology is being deployed today, mainly in low-end applications. As semiconductor processes improve, it will inevitably move into higher-speed designs as well.
Consumer and SOHO

At the low end of the networking market, such as equipment for consumer or SOHO (small office/home office) use, data throughput is typically less than 10Mbps. At these rates, both the control plane and data plane can be handled in software on a CPU running at less than 400MHz. This type of low-cost CPU can be licensed from several sources and integrated into a system-on-a-chip (SoC) device to form the core of a low-cost router or broadband gateway. We do not consider these devices to be SCDP because they do not integrate any data-plane functions, other than perhaps an encryption offload engine.

Throughput requirements are increasing, however, due to the deployment of next-generation broadband technologies such as VDSL, PON, and DOCSIS 3 (cable modem). These technologies can supply from 30Mbps to 100Mbps or more into a home or small office. In addition, 802.11n provides wireless transmission rates of 100Mbps or more. At these data rates, a single CPU engine cannot perform both the control and data planes.

For example, Ikanos offers its Fusiv line of processors, targeting VDSL and PON. These SCDP chips combine a 500MHz MIPS CPU with a set of six custom packet engines that each run at 333MHz. Working together, these programmable packet engines autonomously handle most traffic (including IPSec), involving the CPU only for exception traffic, such as flow setup and teardown. The Fusiv chip can handle 200Mbps of worst-case traffic while leaving most of the main CPU available for application-level processing. Yet the chip sells for less than $25 and is rated at just 2.2W (typical).

Small/Medium Businesses (SMB)

Historically, SMB has used a hodge-podge of network connections, including T1/E1, fractional T3/E3, HDLC, and SHDSL. Many of these connections use the ATM protocol and thus require greater levels of processing to convert them to the TCP/IP protocol used for the internal Ethernet network. SMB equipment typically uses products such as Freescale’s PowerQuicc, which combines a Power CPU with a programmable data-plane engine. This engine handles the data plane, including protocol conversion, while the CPU handles the control plane and application-layer processing.

With these legacy connections falling behind in bandwidth, many small businesses are switching to next-generation broadband links, while medium-size businesses are plugging into carrier Ethernet service at 100Mbps or even 1Gbps. Although these new services use TCP/IP, eliminating the protocol conversion, their data rates are much greater than in the past. As a result, many SMB products continue to use an SCDP design.

For example, LSI’s APP2200 targets SMB applications with a single chip that combines dual ARM11 CPUs for the control plane and four programmable packet engines for the data plane. The dual 290MHz CPUs can operate in SMP mode and share the control-plane processing; alternatively, one CPU can be reserved for voice processing. The data-plane engines are arranged in a pipeline and optimized for specific tasks (e.g., classification, editing, queuing) to reduce cost and power. LSI’s high-end model supports 3Gbps (worst case) at a price of $120 and a typical power dissipation of 8W.
Communications Infrastructure

Communications infrastructure includes access equipment such as broadband termination equipment (e.g., DSLAM) and cellular infrastructure, plus higher-speed equipment such as edge routers, multiservice switches, and core routers. Today, SCDP technology is most commonly found in access equipment. These systems aggregate a large number of client connections into a single high-speed uplink and often perform protocol conversion as well. The control-plane processor may have additional management responsibilities.

Freescale’s PowerQuicc is a popular choice in these systems. For example, the MPC8360 combines a 667MHz Power CPU with two packet engines running at 500MHz. Working together, these processors can handle 2Gbps of traffic, handling both aggregation and protocol conversion.

Future Opportunities

High-speed equipment, such as edge routers and enterprise routers, typically combines a general-purpose processor for the control plane and an ASIC or network processor for the data plane. These systems often use a modular architecture in which several line cards process incoming traffic while a single central control processor handles the control plane.

An SCDP can be used in line cards to handle certain control-plane tasks, such as exception traffic. This technique offloads the central control processor, which is increasingly overburdened as wire speeds increase, without requiring the entire control-plane software to be decentralized. Even a single line card, however, typically handles 4Gbps to 40Gbps of full-duplex traffic; SCDP chips will initially target the lower end of that range.

An SCDP is also ideal for security appliances. Many systems today combine a high-speed x86 or RISC processor with external coprocessor or accelerator chips. Performance requirements are increasing not only because of wire speeds but also due to the increasing number of security threats and the software required to defend against them (e.g. firewall, intrusion detection/prevention, virus scanning). These systems are starting to adopt products such as Cavium’s Octeon, which combines up to 16 MIPS CPUs with hardware offloads for encryption, pattern matching, data compression, TCP/IP, and packet processing. In this homogeneous architecture, the CPUs can be allocated to the control plane or data plane as needed. Octeon chips range in performance from 600Mbps to 20Gbps and in price from $20 to $900.

Conclusions

The single-chip control/data-plane processor offers many advantages over traditional discrete solutions. Integration improves performance, reduces both chip cost and system cost, and reduces power dissipation, a key limiter in many system designs. Furthermore, an off-the-shelf SCDP simplifies the system-design task and provides a single support contact.
SCDP designs are widely deployed today in consumer, SMB, and access equipment. Although most consumer networking equipment today uses simple system-on-a-chip processors, the shift to next-generation broadband technologies is driving a transition to true SCDP devices in the consumer and SOHO markets. In SMB and access equipment, SCDP chips will evolve to support greater data rates and additional functions.

Ongoing improvements in manufacturing technology are enabling the newest SCDP products to achieve performance levels of 10Gbps and above. These performance levels enable greater usage of SCDP in enterprise and metro equipment, both in appliances and line-card designs. Homogeneous SCDP are being adopted in security equipment, where their general-purpose CPUs are suited to complex data-plane processing.

For OEMs that develop equipment for multiple markets, the ideal SCDP is a member of a broad family of software-compatible devices. In this scenario, an OEM can port its control-plane and data-plane software to the SCDP and use various family members in different platforms. This scalability will minimize the OEM’s software efforts and enable rapid deployment of new systems.

SCDP technology is well established in networking equipment today. Moore’s Law improvements are driving SCDP into systems with data rates of 10Gbps and above. These SCDP devices use multicore technology to deliver high levels of performance at moderate cost and power levels. OEMs should analyze the benefits of this technology at all but the highest levels of data-plane throughput.

Linley Gwennap is founder and principal analyst of The Linley Group and coauthor of “A Guide to High-Speed Embedded Processors” and “A Guide to Network Processors.” The Linley Group offers the most comprehensive analysis of the networking-silicon industry. We analyze not only the business strategy but also the technology inside all the announced products. Our in-depth reports covers topics including network processors, content processors, general-purpose CPUs, security processors, and communications processors. For more information, see our web site at www.linleygroup.com.