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*A strong processor is worthless if it can't run your application or requires you to expend inordinate amount of resources to rewrite your application. Thus the value of the processor depends on the underlying ecosystem and its software compatibility. AMD's new EPYC processor family delivers backward compatibility with a large installed base of server applications and third-party peripherals and adapters. In addition to being fully compatible with the x86 register set, EPYC supports all existing Broadwell instructions. Customers can enhance system performance by tuning their software for the underlying hardware, as they would do for any new x86 processor.*

AMD's EPYC processors open a new era of server-processor competition that has been absent for some time, a lack of competition that shut out innovation from many system developers. We expect AMD to offer seamless x86 compatibility with EPYC, which also offers high integration with existing x86 solutions in the market. The increased competitive landscape will enable OEMs to add their innovation into the server platform. End users should benefit from a competitive environment that will foster innovation and provide customer choice. EPYC promises performance and power efficiency to rival mainstream x86 processors currently shipping.

A major element of cost effectiveness is backward compatibility with the existing infrastructure of x86 applications and third-party hardware. Without that, customers must invest significant resources to develop or port software to the new platform. AMD's decades of x86 development grant it a unique ability to deliver software and hardware compatibility.

Compatibility allows customers to easily port software between platforms. In many cases a customer can simply move a software image between platforms. Often, new processors add instructions and capabilities that are not exercised by existing infrastructure but these must be tested to not cause problems to existing applications. Thus, compatibility with the installed base of x86 platforms is not a given but must be designed and validated into a new processors. This white paper looks at the EPYC processor family and AMD's validation programs to ensure backward compatibility. Specifically, it lists the similarities between the EPYC processors and Intel's mainstream Xeon processors and discusses the impact of the few differences.

## *EPYC and Xeon Similarities*

AMD has developed and sold x86 processors for decades proving its ability to ship processors that are compatible with the x86 register set. This compatibility allows AMD processors to support all operating systems developed for x86. As with most new processors, EPYC has hardware changes that are handled in the BIOS, but these are not visible to the OS. EPYC's first compatibility challenge is to support the evolving x86 instruction set. Fortunately, EPYC builds upon AMD's earlier server

 

processors, including the Bulldozer and Piledriver, families, which have shown x86 compatibility through high-volume shipments over many years.

Piledriver, AMD's previous-generation CPU, launched in 4Q'12 and supports most of the instructions enabled in Intel's Haswell-based Xeon E5 processors that were available at the same time. Since then, Intel has updated its processors with the Broadwell microarchitecture and in 2017 plans to announce next-generation Xeon E5 processors based on the Skylake microarchitecture. Table 1 shows the instructions supported on EPYC and the new instructions expected on the Skylake-based Xeon E5 processors.

| Instruction | Description | EPYC | Broadwell | Skylake * |
|---|---|---|---|---|
| ADX | Extended multi-precision arithmetic | ✓ | ✓ | ✓ |
| AVX 1.0 | New vector, 256 bit instructions | ✓ | ✓ | ✓ |
| AVX 2.0 | Additional vector, 512 bit instructions | | ✓ | ✓ |
| BMI1 | Bit manipulation instructions | ✓ | ✓ | ✓ |
| BMI2 | Bit manipulation instructions | ✓ | ✓ | ✓ |
| CLFLUSHOPT | CLFLUSH ordered by SFENCE | ✓ | | ✓ |
| CLZERO | Clear cache line | ✓ | | |
| FMA3 | 3 operand fused-multiply-accumulate | ✓ | ✓ | ✓ |
| FMA4 | 4 operand fused-multiply-accumulate | ✓ | | |
| FSGSBASE | Read or write the FS or GS BASE registers | ✓ | ✓ | ✓ |
| F16C | 16 bit floating point conversion | ✓ | ✓ | ✓ |
| MOVBE | Useful for big-endian to little-endian swaps | ✓ | ✓ | ✓ |
| RDRAND | Random number generation | ✓ | ✓ | ✓ |
| RDSEED | Complement to RDRAND random number generation | ✓ | ✓ | ✓ |
| SHA1 / | Secure hash instructions | ✓ | | ✓ |
| SMAP | Supervisor Mode Access Prevention | ✓ | ✓ | ✓ |
| SMEP | Secure Mode Execution Protection | ✓ | ✓ | ✓ |
| SSE4.1, 4.2 | Additional SSE instructions | ✓ | ✓ | ✓ |
| | | | | |
| XSAVE | Saves YMM (256 bit) register state | ✓ | ✓ | ✓ |
| XSAVEC/S, XRSTORS | New Compact and Supervisor Save/Restore | ✓ | | ✓ |
| XSAVEOPT | Speeds XSAVE during context switch | ✓ | ✓ | ✓ |
| TSX | | | | ✓ |
| MPX | | | | ✓ |

**Table 1. Comparing new instructions in EPYC and Skylake.** AMD's new EPYC processor supports all x86 instructions and extensions in Intel's Broadwell products as well as some features of the upcoming Skylake-EP products. *expected instruction in Intel's upcoming Skylake server processor. (Source: AMD and Intel)

Table 1 also shows all of the major instructions supported on AMD's EPYC server processors. EPYC has added several new instructions to Piledriver's proven set. These

new instructions include CLFLUSHOPT, RDSEED, SHA1/SHA256, SMAP, SMEP, and XSAVEC/XRSTORS. CLFUSHOPT flushes multiple cache lines in parallel within a single's processors instruction stream. RDSEED supplements the earlier RDRAND instruction by seeding a nondeterministic software pseudorandom-number generator and complies with the newer SP 800-90B and 800-90C standards. SHA1/SHA256 assist with the calculation of the message and digest of these secure hash algorithms. SMEP prevents supervisor mode execution from user pages and SMAP prevents unintended supervisor mode accesses to data on user pages. XSAVEC/XRSTORS save or restore the states of internal registers such as XMM and YMM to or from memory.

These instructions update EPYC to match all instructions found on current and most in the next generation Xeon E5 processors. As Table 1 shows, AMD is also discontinuing some AMD-specific instructions from its previous generation server processors to help with software portability across AMD and Intel's server platforms.

## *EPYC Differences to Xeon- Skylake*

After AMD started the EPYC development, Intel added new instructions into the server versions of its Skylake processors. Not supported in EPYC, these instructions include AVX512, SGX (Software Guard Extensions) and MPX (Memory Protection Extensions). AMD supports the current AVX 256 bit instructions; AVX512 doubles processing speed for vector operations by doubling the width of internal registers and we expect these to be used in HPC applications. SGX creates a secure execution environment within an application by creating a secure section of memory. The secure memory is encrypted to prevent malware from changing or reading the secure code or data. MPX prevents the data pointer from going past the end of an array; these instructions are typically removed after debugging to optimize performance.

Any software using AVX512, SGX, or MPX instructions will not run on EPYC without being recompiled. Since Skylake-based servers will not ship until 2H17, all current production applications operate without these instructions. Even after Skylake begins shipping, most commercial applications will support the current Broadwell instruction set, as that will dominate the installed base for the next few years. Over time, however, the lack of AVX512 will exclude EPYC from some emerging HPC applications. MPX, which is used for debugging, is likely to be disabled in production software; thus, the lack of MPX support will have minimal impact on E{YC.

For securing memory, AMD and Intel have chosen different paths. Intel requires independent software developers (ISVs) to change their applications and use the SGX instruction. Instead of using new instructions, AMD has implemented a solution rooted in the SoC hardware, that provides secure memory encryption and virtual machine (VM) isolation. This solution does not require any changes to applications, however, there are changes required at the operating system and hypervisor level. AMD is working with Operating System vendors to enable this solution for EPYC. Because these features are implemented in hardware and require no modification to applications, enterprises and CSPs can isolate VM's and securely encrypt memory enabling an extra layer of protection against attacks, even for existing applications. AMD has already upstreamed these code changes for Linux and made them available to the open source

 

community. This functionality should be available for testing in 2H17, and AMD expects it to be included in commercial distributions in 2018. The company is also working with Microsoft to incorporate the required changes in Windows. More detailed information about AMD's security implementation can be found at http://amd-dev.wpengine.netdna-cdn.com/wordpress/media/2013/12/AMD_Memory_Encryption_Whitepaper_v7-Public.pdf.

EPYC and Xeon have other hardware differences that will not impact compatibility but may affect the performance of the two platforms. These differences include the number of threads, cache size and bandwidth, level of integration, and memory bandwidth. Implications of these are discussed further in the "EPYC: Designed for Effective Performance" white paper.

## *Ensuring Compatibility*

EPYC has been validated on all major server operating systems, including Microsoft Server and all of the leading commercial Linux distributions as well as the virtualized versions such as Hyper-V, Linux KVM, VMware, and Citrix XenServer. The OS vendors, along with AMD, validate the EPYC platform on not only the current release of the OS, but also the previous release of that OS. The company also works with the leading OS suppliers to validate EPYC on the pre-release of next-generation OS' to ensure compatibility on the first day of commercial release.

In many cases, the OS supplier will certify the OEM's EPYC platform for compatible operation. AMD provides ongoing support for this compatibility, which is also supported by the OS vendor and the server OEM. The depth of AMD's validation testing can be gauged through the length of its validation program, which aggregates to more than 700 days of testing on the different OS platforms.

For hardware compatibility, AMD's validation program includes testing a broad range of third-party PCI Express add-in cards. These include cards and host-bus adapters (HBAs) for RAID, Fibre Channel, SAS/SATA, NVMe, InfiniBand, networking, and graphics. The company validates add-in cards from multiple suppliers for these functions. Its validation includes physical (voltage and temperature) corner cases as well as compatibility on various software stacks. AMD has and will conduct ongoing plugfests where third parties can verify add-in card interoperability with EPYC platforms from multiple suppliers.

AMD validates its processors with DDR4 DIMMs from market leaders such as Samsung, Micron, and HK Hynix. For storage, AMD's validation program includes testing EPYC platform-level compatibility with SSDs and HDD from the leading suppliers. For the PCIe adapters and storage drives, AMD also validates hot-plug operation, which allows users to replace storage drives in live systems.

AMD is working with the industry at large to ensure application compatibility on high volume servers. The company enables application validation by offering reference platform to independent software vendors (ISVs). It also tests operation using software

stacks that include a range of popular applications. As needed, AMD additionally coordinates interoperability validation of applications from ISVs on servers from the leading OEMs.

## *EPYC Hardened For Deployment*

AMD has a long history of shipping x86-compatible server processors. EPYC, its latest rendition, carries on this legacy with the addition of new instructions to match those found on Intel's currently shipping Broadwell-based Xeon processors. The company has a broad and deep validation program to ensure compatibility to the installed base of applications and third party add on hardware. In addition, it has worked with leading equipment vendors to ensure that their software stacks and board adapters are compatible and interoperable on EPYC platforms. The company is also working with the leading OS vendors to ensure compatibility on upcoming releases. Thus, customers can easily migrate their existing workloads and software images to the new EPYC platforms and have the peace of mind for future compatibility.

Many cloud service providers and enterprises implement virtualization to sell virtual machines (VMs) or maximize server utilization. Driven by the need for innovation and greater flexibility, both of these organizations want to have data centers that can use servers with either Intel or AMD processors. This desire will create an environment where VMs must migrate between Intel processors and AMD processors. AMD currently does not support VM migration from EPYC to Xeon processors. But some third parties, such as Visions Solutions, offer tools and support to enable VM migration across different platforms.

The server industry continues to evolve by adding new capabilities and instructions such as AVX512, which promise greater performance for certain HPC applications that take advantage of wide vectors. AMD chose not to optimize the first-generation EPYC for these specialized applications. In addition, Intel and AMD are taking different approaches for security. While Intel requires ISVs to change their applications to implement its latest security features, AMD has decided to instead work with the operating-system vendors to enable security features without forcing changes to the application. This approach will result in seamless application support.

EPYC creates a more competitive server-processor market, which should reduce equipment prices and potentially translate into lower prices for services offered by cloud service providers. In addition, EPYC increases the diversity of processor options, leading to a more open platform that will be more cost effective while supporting the large installed base of x86 applications.

*This is an AMD sponsored white paper. Jag Bolaria is principal analyst at The Linley Group focusing on server processors, cloud computing and embedded processors. The Linley Group offers the most comprehensive analysis of microprocessor and SoC design. We analyze not only the business strategy but also the internal technology. Our in-depth reports also cover topics including server processors, embedded processors, IoT processors, and processor IP cores. For more information, see our web site at www.linleygroup.com.*